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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,899	10/12/2004	**Huajie Chen**	FIS920040107US1	5898

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FREDERICK W. GIBB, III
Gibb & Rahman, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,899	CHEN ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,9,11-14 and 35-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,9,11-14 and 35-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hite (US pat 4863878).

With respect to claim 8, Hite et al. teach a field effect transistor comprising (see figs. 1A-1D and 2A-2D and associated text):

A silicon substrate 1, wherein the top surface of said silicon substrate has an oxygen content comprising an amount below which would prevent epitaxial growth;

A silicon halo layer 5 on said top surface of said silicon substrate;

A silicon source/drain layer 7 on said silicon halo layer; and

A gate stack 13 above said silicon source/drain layer.

Further with respect to claim 8, since Hite et al. teach the claimed structure, the amount of oxygen content would substantially inherently limit dopants within the silicon layer **and the silicon source/drain layer** from moving into said silicon substrate.

Further with respect to claim 1, how the silicon halo layer and silicon source/drain layer are formed, that is epitaxial growth, has not been given patentable weight since claim is directed to a device.

With respect to claim 9, Hite et al. further teach the source/drain dopants are substantially limited to the silicon source/drain layer. See figs. 1A-1D and 2A-2D and associated text.

Claims 35, 37, 38, and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Hite et al. (US pat 4,863,878).

With respect to claim 35, Hite et al. teach a field effect transistor comprising (see figs. 1A-1D and 2A-2D and associated text):

A silicon substrate 1;

wherein the top surface of said silicon substrate has an oxygen content 3 comprising an amount below which would prevent epitaxial growth from said silicon substrate (see epitaxial layer 7 or 9 or 27 is able to grow thereon);

A silicon layer 9 directly on said top surface of the silicon substrate, the silicon layer comprising dopants (source/drain);

Wherein said dopants inherently are substantially limited to said silicon layer by said amount of oxygen content 3 of said top surface of said silicon substrate.

With respect to claim 37, Hite et al. further teach the amount of oxygen content would inherently limit said dopants within the silicon layer from moving into the silicon substrate.

With respect to claim 38, Hite et al. further teach the silicon is doped with source/drain dopants. Further, how the silicon layer is formed has not been given patentable weight since claim is directed to a device.

With respect to claim 39, Hite et al. further teach source/drain regions are formed in the silicon layer.

Claims 42, 43, and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Hite et al. (US pat 4,863,878).

With respect to claim 42, Hite et al. teach a field effect transistor comprising (see figs. 1A-1D and 2A-2D and associated text):

A silicon substrate 1;

wherein the top surface of said silicon substrate has an oxygen content 3 comprising an amount below which would prevent epitaxial growth from said silicon substrate (see epitaxial layer 7 or 9 or 27 is able to grow thereon);

wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth (see epitaxial layer 7 or 27 is able to grow thereon);

A silicon source/drain layer 9 directly on said top surface of the silicon substrate 1 having oxygen content 3 the silicon layer comprising source/drain dopants;

Wherein said source/drain dopants inherently are substantially limited to said silicon layer by the amount of oxygen content 3 of said top surface of said silicon substrate.

With respect to claim 43, Hite et al. further teach the amount of oxygen content would inherently limit said source/drain dopants within the silicon layer from moving into the silicon substrate.

With respect to claim 46, Hite et al. further teach the silicon is doped with source/drain dopants. Further, how the silicon layer is formed has not been given patentable weight since claim is directed to a device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hite et al. (US pat 4,863,878) as applied to claims 8 and 9 above, and further in view of Thompson et al. (US pat 6,020,244) and Noguchi et al. (US pub 2004/0135210).

With respect to claim 12, Hite et al. fail to teach doping the silicon source/drain layer with halo dopants that are different from source/drain dopants.

Thompson et al. teach doping halo dopants that are different from source/drain dopants into a silicon source/drain layer to achieve reduction in leakage current and improvement in punchthrough characteristics. See fig. 1 and associated text and col. 4, lines 35-45.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Thompson et al. into the device of Hite et al. to attain the above benefit.

With respect to claim 14, Hite et al. further teach the top surface of the silicon substrate is essentially damaged (see claims) but fail to teach removing native oxide from the silicon substrate.

However, the removal of unwanted native oxide from a surface of silicon substrate is well-known.

With respect to claims 11 and 13, Hite et al. fail to teach a column portion or trench having isolation extending from below the gate and through the silicon halo layer and silicon source/drain layers.

Noguchi et al. forming a column portion or trench having isolation 51 extending from below a gate 73 and through a silicon source/drain layer 24
a silicon halo layer 26 to prevent unwanted interaction between devices. See fig. 5 and associated text.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Noguchi et al. into the device of Hite et al. to attain the above benefit.

Claims 36, 40, and 41 rejected under 35 U.S.C. 103(a) as being unpatentable over Hite et al. (US pat 4,863,878) as applied to claims 35, 37, 38, and 39 above, and further in view of Thompson et al. (US pat 6,020,244) and Noguchi et al. (US pub 2004/0135210).

With respect to claim 36, Hite et al. fail to teach doping the silicon layer with halo dopants that are different from source/drain dopants.

Thompson et al. teach doping halo dopants that are different from source/drain dopants into a silicon source/drain layer to achieve reduction in leakage current and improvement in punchthrough characteristics. See fig. 1 and associated text and col. 4, lines 35-45.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Thompson et al. into the device of Hite et al. to attain the above benefit.

With respect to claim 40, Hite et al. fail to teach forming isolation regions in the substrate or silicon source/drain layer.

However, the formation of isolation regions a silicon substrate and a silicon layer for the purpose of electrically isolation is well-known in semiconductor art.

With respect to claim 41, Hite et al. further teach the top surface of the silicon substrate is essentially damaged (see claims) but fail to teach removing native oxide from the silicon substrate.

However, the removal of unwanted native oxide from a surface of silicon substrate is well-known.

Claims 44, 45, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hite et al. (US pat 4,863,878) as applied to claims 42, 43, and 46 above, and further in view of Noguchi et al. (US pub 2004/0135210).

With respect to claim 44, Hite et al. fail to teach a column portion or trench having isolation extending from below the gate and through the silicon halo layer and silicon source/drain layers.

Noguchi et al. forming a column portion or trench having isolation 51 extending from below a gate 73 and through a silicon source/drain layer 24
a silicon halo layer 26 to prevent unwanted interaction between devices. See fig. 5 and associated text.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Noguchi et al. into the device of Hite et al. to attain the above benefit.

With respect to claim 47, Hite et al. fail to teach forming isolation regions in the substrate or silicon source/drain layer.

However, the formation of isolation regions a silicon substrate and a silicon layer for the purpose of electrically isolation is well-known in semiconductor art.

With respect to claim 45, Hite et al. further teach the top surface of the silicon substrate is essentially damaged (see claims) but fail to teach removing native oxide from the silicon substrate.

However, the removal of unwanted native oxide from a surface of silicon substrate is well-known.

Response to Arguments

Applicant's arguments with respect to claims 8-9, 11-14, and 35-47 have been considered but are moot in view of the new ground(s) of rejection.

In response to the applicant's arguments in the paragraphs on pages 7-9 of the amendment dated 05/18/07, it is submitted that a comparison of the recited process with the prior art process does not serve to resolve the issue concerning patentability of the product. In re Fessman, 489 F2d 742, 180 uspq 324 (CCPA 1974). Where a product is patentable depends on whether it is known in the art or it is obvious, and is not governed by whether the process by which is made is patentable. In re Klug, 333 F2d 905, 142 uspq (CCPA 1964). In an exparte case, product by process claims are not constructed as being limited to the product formed by the specific process recited. In re Hirao et al., 535 F2d 67, 190 uspq 15, see footnote 3 (CCPA 1976).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Long Pham/
Primary Examiner, Art Unit 2814

/L. P./